

METHOD OF ESTABLISHING A PWM-MODULATED OUTPUT SIGNAL REPRESENTATION

Field of the invention

- 5 The invention relates to a method of establishing a PWM modulated output signal representation (OS) according to claim 1.

Background of the invention

- 10 Pulse width modulation, PWM, is used widely within the field of for instance audio amplifiers. Generally, the available pulse width modulation techniques may be categorized into typically three different types of modulation, natural pulse width modulation, NPWM, uniform pulse width modulation, UPWM or linearized pulse width modulation, hereinafter LPWM.
- 15 Generally, all pulse width modulation implies the technique of transforming or converting an input signal into an output square wave signal having a certain pulse width, at least partly defined by the input signal by comparison of the input signal to a reference signal.
- 20 A short review of the general understanding of the above-mentioned groups of pulse width modulation techniques will be given below.
- Natural pulse width modulation, NPWM, typically implies the comparison of a continuous time signal, typically an analogue waveform signal, to a reference signal, typically a sawtooth signal. The output signals will then switch between typically two output levels when the input signal and the reference signal intersect.
- The natural pulse width modulation technique, NPWM, is generally regarded as distortion free within the audio band.

Uniform pulse width modulation, UPWM, typically implies the comparison of a discrete time signal, typically a digital waveform signal such as a PCM signal, to a reference signal, typically a sawtooth signal. The output signals will then switch between typically two output levels when the input signal and the reference signal intersect. A well-known problem related to uniform pulse width modulation, UPWM, is that the input signal, due to its discrete nature, may basically not necessarily be represented at the time of intersection. This problem may be dealt with in different ways, e.g. simply by accepting the error and quantizing the intersection time according to a quantizing algorithm.

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In order to counteract the inherent distortion, several PWM linearization techniques have been disclosed within the art.

Linearized pulse width modulation, LPWM, typically deals with emulation of the theoretical value of the input signal, if a sample of the input signal was actually present at the time of intersection between the reference signal and the input signal.

Such methods are often referred to as linearized pulse width modulation, LPWM. Prior art demonstrates linear interpolation between two adjacent input samples to achieve the output pulse width. In other words, the linearization algorithms typically operate on more than one sample of the input signal to determine the linearized output pulse width.

Thus several linearization techniques apply to first order interpolation of the input signal between the discrete samples in order to estimate the true cross point between the input signal and the reference signal.

Other techniques implying 2nd order interpolation have been applied for the purpose of coming closer to the "true" cross point, thereby minimizing the resultant harmonic distortion.

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A problem of many of the relatively new and improved LPWM techniques is that the resulting improvement is relatively costly with respect to computing requirements. Thus, several linearized pulse width modulation techniques require division.

5 Typically, prior art LPWM-techniques either do not include an algorithm to determine the pulse width, or they disadvantageously use a division operation to compute the pulse width. Division operations are relatively computationally inefficient in digital signal processing and require many more computation steps than
10 therefore required to implement techniques involving division. Generally known implementations do not provide computationally efficient methods to reduce harmonic distortion in pulse width modulated systems.

It is an object of the invention to provide a method, which may be applied in a PWM
15 modulation technique featuring low distortion and computationally efficiency.

Summary of the invention

The invention relates to a method of establishing a PWM-modulated output signal representation (OS),

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providing a stream of parallelly determined intersection representations (PIR) on the basis of a stream of parallel reference signal representations (PRSR) and an input signal (IS),

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establishing a serial PWM output signal representation (OS) by transforming said stream of parallelly determined intersection representations (PIR) into a stream of serial intersection representations (SIR) by means of a relative time shift of at least one of said parallelly determined intersections (PIR).

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According to an embodiment of the invention, an advantageous way of providing intersection estimates has been obtained, as each or at least a number of intersection

estimates between a reference signal may be established partially while taking only the individual partial reference functions into consideration.

The partial reference signals may also within the scope of the invention be referred to
5 as parallel reference signal representation.

It is noted that a stream of parallel reference signal representations (PRSR) may both refer to a physical real signal or, preferably, a representation of a desired reference signal.

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It is noted that the phrase parallelly determined intersection representation primarily relates to a desired reference signal, which has been modified, primarily by a time transformation, into a number of signal representations, having advantageous properties with respect to subsequent signal processing. In particular, an
15 advantageous property may refer to that of transforming a reference signal representation into signal representations, which may each relatively easily be solved when determining intersections between an input signal and the reference signal components. This advantageous reference signal representation may also be understood as a "packed" reference signal, which when being packed may undergo
20 processing, e.g. for the purpose of comparing the reference signal representation to an input signal representation, and then afterwards may be "unpacked" by a relatively simple "unpacking-technique", which when applied maintains or substantially maintains the information obtained during the processing on the basis of the "packed" signal representation.

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A further property of the handling a the parallelly determined intersections representation is that it may be dealt with truly parallel, i.e. by performing the computing related to each part of the parallel representation in parallel. It should, however, be emphasized that the computing related to the finding and transformation
30 of intersections may also be performed serially if desired, i.e. one by one.

It is noted that the stream of serial intersection representations itself may be represented in various representation containing formats, serial or parallel. However, even though the representation may be held in a kind of parallel representation, the serial intersection representations will refer to a serial time base.

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According to an embodiment of the invention, the intended reference signal may be kept in a parallel signal representation, according to which the different parallel signal representations forming the complete reference signal may be kept in an advantageous representation. In other words, the intended signal, e.g. a double-sided
10 triangular reference signal may be established as two parallel linear functions, one function representing the linear rising part of the triangle wave the other function representing the falling linear triangular wave of the reference function. In this way, the different parts of the complete signal may be transformed into a function, which may independently be compared to the input signal. An example of such
15 advantageous representation is to transform the time axis of the two "independent" functions by simply adding and subtracting a delay, thereby obtaining that both of the parallel symmetrical functions are symmetrical with respect to time=0. In this way, an intersection may be determined in a relatively simple manner, as the necessary mathematical computing may be simplified when the function is
20 symmetrical. Subsequently, the established intersection estimates may be transformed by applying more or less complex transformation algorithms. It should, however, be noted that the transformation may typically be performed by a transformation in time which is substantial compared to the period of the intended reference signal.

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According to an embodiment of the invention the established resulting - global - time shift may in principle be any time shift equal or greater than zero. It is, however, noted that the time shift, depending on how the calculations are analyzed, may in fact be regarded as negative if each time estimate is automatically delayed by a
30 predefined initial delay in order to facilitate steady computing. If this is the case, as it typically is, the effective and principal idea of applying the time transformation

scheme is to apply a certain offset between a number of determined intersection estimates, thereby offering the system to establish and perform the main processing in another time domain than the resulting serial true time PWM signal.

- 5 According to an embodiment of the invention, the parallel reference signal may be computed in different time domains and subsequently transformed into one common time domain.

According to an embodiment of the invention, the term PWM refers broadly to
10 different types and variants of PWM modulation techniques, e.g. NPWM, LPWM, UPWM or e.g. pulse position modulation, i.e. wherever a pulse must be shifted according to a predefined modulation technique.

In an embodiment of the invention, the PWM-modulated output signal representation
15 (OS) is established according to a time transformation scheme.

According to an embodiment of the invention a time transformation scheme may advantageously be applied for converting a time estimate determined in one domain into corresponding intersection estimate in another domain. The time transformation
20 scheme may generally comprise very straightforward time transformations, e.g. by applying simple addition and subtracting by a fixed time representation value. However, more complex time transformation schemes may be applied.

In an embodiment of the invention, said time transformation scheme determines a
25 serial stream of intersection estimates (SIR) and whereby said serial stream comprises frames of a predetermined number of PWM determining estimates.

According to an advantageous embodiment of the invention, the serial stream of intersection estimates may be regarded as frames of intersections, where the
30 individual frames determine the combined properties a corresponding period of a intended reference signal.

In an embodiment of the invention, at least one of said predetermined number of PWM determining estimates is established on the basis of a corresponding first parallel intersection estimate being modified by a first time shift and where at least
5 one further of said predetermined number of PWM determining estimates is established on the basis of a further corresponding parallel intersection estimate being modified by a further time shift differing from said first time shift.

In an embodiment of the invention, said first time shift is obtained by adding ΔT to
10 said first parallel intersection estimate, said further time shift is obtained by subtracting ΔT from said further parallel intersection estimate and where said established time shifted intersection estimates result in a first PWM output signal.

In an embodiment of the invention, a further PWM output signal is obtained by
15 establishing a first differential time shift by subtracting ΔT from said first parallel intersection estimate and establishing a further differential time shift by adding ΔT to said further parallel intersection estimate and where said established time shifted intersection estimates result in a further PWM output signal.

20 In an embodiment of the invention, said parallel reference signal representations (PRSR) comprise two geometrically linear functions and where said time transformation scheme is applied for subjecting intersection estimates obtained between said two linear functions and the input signal representation (IS) to two different time shifts, thereby transforming said intersection estimates into
25 intersection estimates referring to the same time base.

In an embodiment of the invention, said parallel reference signal representations (PRSR) comprise two functions, preferably linear, and where said time transformation scheme is applied for subjecting intersection estimates obtained
30 between said two functions and a differential input signal representation (IS) to four time shifts, at least two of said four shifts being mutually different, thereby

transforming said intersection estimates into intersection estimates referring to the same time base.

5 In an embodiment of the invention, a three-level output signal is obtained by determining four intersections referring to different time bases and subsequently transforming these intersections into corresponding intersections referring to the same time base according to said time transformation scheme.

10 In an embodiment of the invention, a three-level output signal is obtained by determining two intersections between a parallel reference signal representation (PRSR) of a double-sided triangular reference signal and an input signal representation (ISR),

15 transforming said two determined intersections into four intersection representations by four time shifts.

In an embodiment of the invention, said input signal representation comprises a single-ended input.

20 In an embodiment of the invention, said input signal representation comprises a differential input.

In an embodiment of the invention, said input signal (IS) is digitally represented.

25 In an embodiment of the invention, said stream of parallel reference signal representations (PRSR) is established as functions having desired properties with respect to the time axis.

30 In an embodiment of the invention, said stream of parallel reference signal representations (PRSR) is established on the basis of a model function (MF), which is represented in at least two different domains having mutually different time bases,

one part of the model function (MF) being represented in a first domain and at least one further part being represented in a further domain.

In an embodiment of the invention, said model function (MF) is a double-sided
5 triangular periodic signal.

Figures

The invention will now be described with reference to the figures of which

- Fig. 1 illustrates the principles of an advantageous embodiment of the invention,
- Fig. 2 illustrates the principles of a parallel and serial domain according to an embodiment of the invention,
- Fig. 3 illustrates the principle of double-sided PWM modulation,
- Fig. 4 illustrates a model signal of a desired effective reference signal,
- Fig. 5 illustrates the principle of determining intersections in one domain and transforming the obtained result into another domain,
- Fig. 6 illustrates an application of the invention,
- Fig. 7 and 8 illustrate the obtained result of a double-sided PWM according to an embodiment of the invention,
- Fig. 9 illustrates the principles of three-level differential PWM according to a preferred embodiment of the invention,
- Fig. 10 and 11 illustrate the obtained result of a three-level double-sided PWM according to a preferred embodiment of the invention,
- Fig. 12-14 illustrate various embodiments of the invention,
- Fig. 15 and 16 pinpoint the single transformation steps according to a preferred embodiment of the invention,
- Fig. 17 illustrates an applicable counter-based PWM pulse generator and
- Fig. 18 illustrates a differential implementation of the invention.

Detailed description

Basically, the invention may be applied in different technical contexts, as it will be described below.

5 A typical application may be a PWM amplifier or converter (PWM: Pulse width modulation), where the input signal is compared to a reference signal, physically or digitally represented, and where the comparisons result in a stream of pulse width modulated output signals. This application, in itself known within the art, may therefore be subject to several modifications with respect to e.g. handling of input
10 signals, establishment of intersections between input and reference signal(s) and in particular with respect to the output stage where output edges are created on the basis of the final determined edges. This stage may be subjected to several different noise shaping techniques in order to for example compensate the relatively restricted possibilities of obtaining high-quality signals by available high or small signal
15 electronics.

Fig. 1 illustrates the principles of an advantageous embodiment of the invention.

Starting from the left, an input signal IS is fed to the intersection determining block
20 10 of a signal processing circuit according to an embodiment of the invention. The intersection-determining block 10 also receives a reference signal representation PRSR referred to in the following as a parallel signal representation. This will be described in detail below with reference to fig. 2. It should, however, be noted that the illustrated block diagram should not be confused with the physical topology of a
25 physical circuit according to the principles of the invention. As an example, the illustrated reference signal representation PRSR may typically be established internally in the intersection block 10. In other words, according to an embodiment of the invention several modifications may be applied with respect to the current and other illustrations as long as the basic ideas of the invention are complied with.

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The input signal is compared to two or more separate reference signal representations forming the complete reference signal representation PRSR and results in a corresponding number of parallel intersection estimate representations PIR. Although referred to as parallel, it should be emphasized that the way of representing the intersection estimate representations may vary from application to application, e.g. as
5 a serial stream of intersection estimates. The term parallel in this context basically serves to highlight the origin of the determined intersection estimates, namely the basic parallel separation of two or more comparisons.

10 Moreover, it should be emphasized that the phrasing of parallel signal or representations does not necessarily refer to processes or streams, which are strictly processed at the same time. This may of course happen according to variants of the invention, but the expression parallel rather covers separate handling and processing of the representations.

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The parallelly processed intersection estimates will then be fed to a domain-transforming block 11. The domain-transforming block 11 transforms incoming parallel intersection estimates PIR into intersection estimates referring to a common time base, i.e. a serial stream of intersection estimates SIR.

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Again, the term serial stream should not be confused with requirements of keeping the intersection information in one single stream, but rather that the intersection estimates now refer to a common time base and may therefore directly or in a modified way be converted or result in the establishment of a PWM output signal.

25 Hence, the serial stream of intersection estimates SIR may in fact be kept in one or several signal processing formats.

It should in this context be noted that different necessary processing, such as noise shaping, may also be included in the domain-transforming block 11.

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The function of the time domain-transforming block 11 is primarily to bring the established intersection estimates PIR into one or multidimensional serial stream SIR of intersection estimates referring to the same time base. This may be done in several different ways according to a time transformation scheme by establishing a relative alignment in time between the parallel streams of intersection estimates PIR. The relative alignment in time may e.g. be established by a time shift, positive or negative to one or more predetermined strings of the parallel intersection estimates, thereby establishing an effective relative alignment in time between the previously established intersection estimates. This relative alignment has the effect of transforming the parallelly determined intersection estimates into a common time base, which may subsequently be more or less straightforwardly converted into a PWM output.

The above-mentioned time shift may be fixed or may on a real-time basis be established according to a predefined time shift determining function.

The serial intersection estimates SIR are then fed to a converter 12, which may then convert the intersection estimates into serial output signals OS, i.e. a single or multistream signals referring to the same time base.

It is noted from the above that a transformation from one domain into another of the intersection estimates may simply be performed by a fixed or varied adding or subtraction of time. According to a very preferred embodiment of the invention, this transformation may simply be performed by adding or subtracting of fixed time shift, namely time shift corresponding, with opposite sign, to the delays applied for transforming a model reference signal into the parallel reference signal representation PRSR.

Basically, a parallel reference signal representation PRSR represents a signal, which may be somewhat more complex in nature compared to e.g. traditional sawtooth reference signals of PWM amplifiers. The parallel representation may comprise two

or more partial reference signal components, together representing a complete reference signal property of a desired reference signal model.

According to an embodiment of the invention, the different partial components of the reference signal representation, representing the desired reference properties may be individually prepared for the intended computing. An example of a preferred preparation of a partial signal is an individual transformation of the time axis of the different partial model components for the purpose of representing the partial representations of the model in a manner suitable for the intended computing, e.g. by transformation of the time axis so that one or preferably all the partial reference signal components are symmetrical with respect to time $t=0$. In this context $t=0$ refers to the centre of a PWM period of a partial reference signal.

It should again here be emphasized that the term parallel refers to a number of partial reference signal representations referring to at least two different time bases, and not to the specific format in which the reference signal representation has been represented in but rather to the nature of the partial signal representations. Evidently, a parallel format or e.g. a time-multiplexed format, i.e. both in parallel or serial streams of signal representing data, may be applied for the purpose within the scope of the invention. This aspect is relevant for all references to parallel or serial computing or data streams.

Fig. 2 illustrates by means of a block diagram a model function MF representing an example of a desired reference signal function, e.g. a triangular double-sided reference signal. The illustrated model function MF may then be divided into a suitable number of partial model functions, also referred to as parallel reference signal representations, representing the characteristics of the desired reference function. This may in practice and preferably be done via an individual time-transformation TT of the intended partial reference signal representations. In case of a double-sided signal, a suitable number of parallel reference signal representations PRSR may be two, e.g. PRSR1 and PRSR2. The time transformation TT1 may

advantageously be applied for the purpose of obtaining a signal representation of the individual parallel reference signal representations PRSR1, PRSR2, PRSR3 and PRSRN, which may advantageously be computed for the desired purpose and the applied time transformation applied is therefore typically different with respect to at
5 least two partial reference signal representations.

It is noted that the above-described establishment of a parallel reference signal representation PRSR1, PRSR2, PRSR3 and PRSRN basically represents one of several methods applicable for the purpose of establishing a desired reference signal
10 representation. Once the parallel reference signal representations PRSR1, PRSR2, PRSR3 and PRSRN have been established, no further considerations regarding the origin of these signals need to be done other than adapting a suitable time transformation TT2 for the purpose of converting the established intersection estimates IE1, IE2, IE3 and IEN into an output signal referring to the same time base.

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It should be noted that the establishment and handling of intersection estimates and the subsequent conversion of these into a signal referring to the same time base may be done in numerous different ways. Thus, a variation with respect to the above-described topology may be used when establishing a differential PWM output signal
20 e.g. with reference to fig. 15 and fig. 16.

Different detailed examples of such embodiments of the invention will be described below.

25 According to an embodiment of the invention, the reference signal representation may for example be obtained by applying a more complicated reference waveform, e.g. a triangular shape instead of a conventional sawtooth, thereby obtaining improvement of the quality of a PWM signal. This shape causes the PWM pulse to have both a start point (which in the sawtooth case is fixed in time) and an end point.

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Such a waveform is illustrated in fig. 3 where an input signal representation ISR is compared with a triangular reference signal RS.

In order to obtain an advantageous handling and computing of the above-illustrated
 5 in the context relatively complex reference signal representation, the x-axis, i.e. the time axis, may be shifted and scaled before the process of determining intersection estimates between the input signal representation and the reference signal representation begins. The reference signal may be set to equal $f(x) = x$ in fig. 4 illustrating a stream of periodic reference signal representations.

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The left side of the triangle may be regarded as a first part of the reference signal representation and the right side of the triangle may be regarded as a second part of the reference signal.

15 A second order model of the input signal representation may be established by means of a polynomial model and may be found as:

$$\begin{bmatrix} p_0 \\ p_1 \\ p_2 \end{bmatrix} = \begin{bmatrix} t(k-1)^0 & t(k-1)^1 & t(k-1)^2 \\ t(k)^0 & t(k)^1 & t(k)^2 \\ t(k+1)^0 & t(k+1)^1 & t(k+1)^2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix}$$

20 It should be noted that several other types of input signal representations may be applied within the scope of the invention, e.g. first, third or higher order polynomials. For the purpose of illustrating some important features and benefits obtained according to an embodiment of the invention, the further explaining is based on a second-order representation a double-sided, i.e. a triangular, reference signal
 25 represented according to an embodiment of the invention as a parallel reference signal.

So the polynomial model using the left slope x-axis, i.e. the first partial reference signal representation, equals:

$$\begin{bmatrix} p_0 \\ p_1 \\ p_2 \end{bmatrix} = \begin{bmatrix} (-3)^0 & (-3)^1 & (-3)^2 \\ (1)^0 & (1)^1 & (1)^2 \\ (5)^0 & (5)^1 & (5)^2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix} = \begin{bmatrix} 5/32 & 15/16 & -3/32 \\ -3/32 & 1/8 & 1/16 \\ 1/32 & -1/16 & 1/32 \end{bmatrix} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix}$$

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And for the right slope, i.e. the second partial reference signal representation:

$$\begin{bmatrix} p_0 \\ p_1 \\ p_2 \end{bmatrix} = \begin{bmatrix} (-5)^0 & (-5)^1 & (-5)^2 \\ (-1)^0 & (-1)^1 & (-1)^2 \\ (3)^0 & (3)^1 & (3)^2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix} = \begin{bmatrix} -3/32 & 15/16 & 5/32 \\ -1/16 & -1/8 & 3/32 \\ 1/32 & -1/16 & 1/32 \end{bmatrix} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix}$$

- 10 As seen in the above, the two transformation matrices are relatively complicated to compute.

And furthermore, the two polynomial models are now asymmetrically located in time in relation to the PCM samples $t(k-1)$, $t(k)$ and $t(k+1)$ on which the model is based.

- 15 This fact introduces a DC error, which rises with the frequency of the input signal

- A way to get rid of the problems of the asymmetrical approach is to shift the left slope of the triangle to the right, and to shift the right slope of the triangle to the left, thus creating an X, followed by a correction on the crosspoint computed, as shown in
 20 fig. 5, also referred to as the X-modulation. With reference to the terms introduced with reference to fig. 1 and fig. 2, the two partial reference signals may individually be transformed by means of two different time shifts in order to establish two parallel reference signal representations, PRSR1 and PRSR2, basically referring to two different time bases. These two parallel reference signal representations, PRSR1 and
 25 PRSR2, may be computed independently for the purpose of determining the

intersection estimates, IE1 and IE2, between the two parallel reference signal representations, PRSR1 and PRSR2, and the input signal representation ISR. Any suitable intersection providing technique may be applied within the scope of the invention. A preferred intersection technique is described in the pending patent
 5 application PCT/DK03/00334.

The intersection estimates IE1 and IE2 may then be transformed according to a time transforming scheme into transformed intersection estimates, TIE1 and TIE2, referring to a common time base. According to an advantageous embodiment of the
 10 invention the applied time transformations may simply by applied time shifts of opposite signs of the time shifts applied for bringing the desired reference signal into the two parallel reference signal representations PRSR1 and PRSR2.

Another way of interpreting fig. 5 is that 1.0 is added to the signal in the PCM
 15 domain, and 1.0 is subtracted in the PWM domain.

To make the slopes in the X equal $f(x) = x$, the only thing needed is to multiply the x-axis with 2. The transformation matrix for the X-modulation is:

$$20 \quad \begin{bmatrix} p_0 \\ p_1 \\ p_2 \end{bmatrix} = \begin{bmatrix} (-4)^0 & (-4)^1 & (-4)^2 \\ (0)^0 & (0)^1 & (0)^2 \\ (4)^0 & (4)^1 & (4)^2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1/8 & 0 & 1/8 \\ 1/32 & -1/16 & 1/32 \end{bmatrix} \cdot \begin{bmatrix} x(k-1) \\ x(k) \\ x(k+1) \end{bmatrix}$$

It is noted that the relatively simple illustrated transformation of one of the two parallel signal representations results in a matrix which now comprises a number of zeros; in this example row one, column one and three and row two, column two.

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In this way, the basic necessary computing on the reference signal(s) may be simplified for the purpose of root solving/finding of intersections between the reference signal and the input signal.

The switch points may in principle now be found according to known principles already applied in e.g. LPWM, e.g. by applying different more or less complicated models of the input signal, e.g. first or higher order polynomials.

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When the switch points based on the simplified parallel reference signals, here: two partial reference signals computed in two different individual time domains, are determined, they may be transformed into a common time domain for the purpose of realizing a PWM signal referring to the same time base.

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According to a preferred embodiment of the invention, the desired switch points may be found simply by modifying the individual switch times by a time transformation equalling the applied time transformation applied when establishing the parallel reference signal representation with an opposite sign.

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In other words, if the first of two parallel reference signals is established on the basis of a time transformation of $+\frac{1}{2}$ and the second is established on the basis of a time transformation of $-\frac{1}{2}$ with respect to the intended reference signal, e.g. a triangular reference signal, the two resulting switch points may be transformed into a common time base simply by subtracting $\frac{1}{2}$ from the first parallel reference signal and adding $\frac{1}{2}$ to the second.

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Other more complex and advanced methods of a transforming into a common time domain may be applied.

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It should in this context be noted that, according a the teaching of the invention, several apparently rough approximations may actually lead to impressing performance when the method is applied in connection with PWM modulation.

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In a typical application, different linearization techniques may compensate more or less for the relatively restricted resolution in time. Different intersection techniques

may be applied within the scope of the invention. Subsequently, the modulation technique according to the present invention teaches that an intersection determined in one domain may actually be transformed more or less directly into another time domain, still with more than acceptable errors. According to an embodiment of the invention, the disclosed technique may even result in reduced distortion when compared with conventional PWM techniques with fewer computations.

Fig. 6 illustrates an example of an application of the present invention. The illustrated system comprises a PWM amplifier/audio system.

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The system comprises an input block 1901 adapted for receipt of a coded audio signal. The input block 1901 branches the input signal into two principle different directions; in one direction for the purpose of converting the information coded in the input signal into a relevant PWM representation and one direction for the purpose of establishing a clock reference signal on the basis of the input signal.

The latter direction is represented by a PLL clock-synchronizing block 1902 referring to a high-frequency oscillator block 1903.

20 The first principle direction starts with the upsampling block 1904 basically transforming the input signal from one sampling frequency representation into an N times higher sampling representation.

The upsampled signal is then fed to an intersection-computing block 1905 adapted for determination of intersections with a parallel reference signal representation according to an embodiment of the invention. The consecutive noise shaping and quantizing block 1906 feeds the established intersections to a time alignment block 1907 according to an embodiment of the invention, where the established intersections are transformed into one common time domain, elsewhere in the application referred to as a serial signal. The transformed signal is then fed to a

PWM pulse generator, in this case a true differential three level generator 1908 referring to the high frequency generator 1903.

5 The resulting PWM signal is then fed to a power stage 1909 and from there via a demodulator 1910 to a loudspeaker 1911.

Evidently, the above-mentioned application only describes one of several applications within the scope of the invention. Examples of straightforward variants according to an embodiment of the invention may e.g. be realized by replacing the
10 above-illustrated blocks 1905, 1906 and 1907, corresponding to 14, by the blocks described and illustrated in the blocks illustrated in fig. 12 and fig. 13.

Fig. 7 and 8 illustrate a comparison between ideal triangle modulation and X-modulation using the sparse polynomial model.

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It is noted that fig. 8 illustrating the above-described method, when compared with an ideal triangle modulation, although advantageous in many aspects, features undesired harmonics.

20 In the following a further embodiment of the invention will be described featuring further advantageous properties. The further embodiment of the invention comprises a three-level PWM modulator, also referred to by some as a true differential PWM.

Establishment of a three-level PWM signal may e.g. be obtained by changing the
25 sign on the input signal or by changing the sign on the reference signal. A nice property of the above-mentioned X-reference signal is that it is symmetrical in both x and y dimension. So actually, implicitly in the original calculation of the intersection between the input and the "original X", the two further intersections needed have already in practice been established. All we have to do is to time shift these
30 intersections.

The above-mentioned shifting is illustrated in fig. 9. It is noted that in practice the three-level PWM signal is obtained more or less “free of charge” simply by applying an opposite time shift in the sense that the more requiring computing is performed when establishing the intersections.

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Fig. 10 and fig. 11 illustrate a comparison between ideal three-level triangle modulation and three-level X-modulation using the sparse polynomial model. It is here noted that the three-level triangle modulation referred to in fig. 11, even when compared with the ideal three-level triangle modulation, exhibits very low distortion and low high-frequency switch energy.

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Fig. 12 to 14 illustrate a further feature of the invention where noise shaping is included in the realization of the PWM circuit.

Fig. 12 illustrates a prior art three-level PWM circuit in which an input signal is compared to two opposite sign reference signals. Four intersections are determined in each period of the reference signal by an intersection computer 120. Each of the established intersections are individually noise shaped by quantizer and noise shaper circuits 121, subsequently feeding a PWM pulse generator 122 outputting a differential PWM output, also referred to as a three-level PWM output.

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Fig. 13 illustrates an embodiment of the invention where an input signal is compared to two opposite sign reference signals represented as a parallel reference signal representation according to an embodiment of the invention. Four intersections are determined in each period of the reference signal by an intersection computer 130. Each of the established intersections are individually noise shaped by quantizer and noise shaper circuits 121 and thereafter shifted in time to the same time domain and finally fed to a PWM pulse generator outputting a differential PWM output, also referred to as a three-level PWM output.

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Fig. 14 illustrates a further and preferred embodiment of the invention where an input signal is compared to two opposite sign reference signals represented as a parallel reference signal representation according to an embodiment of the invention. Two intersections are determined in each period of the reference signal by an intersection computer 140. Each of the two established intersections are individually noise shaped by quantizer and noise shaper circuits 141 and thereafter shifted in time to the same time domain and finally fed to a PWM pulse generator outputting a differential PWM output, also referred to as a three-level PWM output. According to this embodiment, corresponding to the embodiment illustrated according to fig. 8 and 9, the noise shaping is performed only two times per every fourth determined intersection estimate. This advantage reduces the computational costs significantly.

Fig. 15 illustrates the properties of the advantageous three-level differential PWM amplifier according to an embodiment of the invention corresponding to that of fig. 8 and fig. 9 or fig. 14 where, basically, two determined intersection estimates are converted into four intersection estimates with very little computing, e.g. simple time shifts.

It is here noted that this feature moreover results in a simplified noise shaping due to the fact that two found intersections may be noise shaped prior to the transformation into a common time base having four intersections.

The solid line represents the intended reference signal and the broken lines represent the two parallel reference signals representing the applied parallel reference signals, each illustrated in fig. 15a and 15b, respectively.

According to the illustrated embodiment, a found intersection, marked by an "o" AL and AR may be transformed into an intersection marked by an "x" in a common time domain by subtracting ΔT from the found intersection AL thereby obtaining the desired intersection ALc and adding ΔT to a found intersection AR marked by an "o"

in the parallel domain into an intersection AR_c in the common domain marked by an “x”.

For illustrative purposes the resulting errors when transforming the intersection from the parallel domain to a common domain are illustrated as EL and ER , EL representing the resulting error between the left part of the triangle reference signal ER and the input signal and between the right part of the triangle reference signal and the input signal.

Moreover, fig. 15 illustrates an example of a resulting PWM + output signal, when modulating the input signal between a V_{cc} voltage and zero.

Basically, this transformation corresponds to the already described transformation explained with reference to fig. 4 and fig. 5.

In fig. 16, fig. 16a and fig. 16b, the already and above-described found intersections marked by an “o” applied for establishing a resulting PWM output signal. In this context a PWM+ and PWM- output refer to two output signals together forming a differential PWM output signal.

The highlighted intended reference signal is now the mirrored intended reference signal of fig. 15. It is noted that this mirroring of the reference signal while maintaining the input signal basically corresponds to a mirroring of the input signal while maintaining the reference signal.

As illustrated by fig. 16, the differential intersection values may now simply be established by transforming the found intersection BR , corresponding to the already established intersection AL , into an intersection marked by an “x” in a common time domain now by adding ΔT to the found intersection BR thereby obtaining the desired intersection BR_c and now subtracting ΔT from found intersection BL marked by an

“o”, - corresponding to the already found AR -, in the parallel domain into an intersection BLc in the common domain marked by an “x”.

As illustrated above in fig. 15 and fig. 16, the applied ΔT 's are equal. Evidently,
5 different types of compensations relating to e.g. the above-described error signal may be individually applied to the specific found intersections.

Moreover, it is noted that BR equals AL and BL equals AR, thus demonstrating that the desired intersections ALc, ARc, BLc and BRc may in fact be determined on the
10 basis of determination of only two intersections, e.g. AR and AL. This may both lead to the advantage of reducing the computing related to the determination of intersections significantly, basically from four to two in this specific embodiment of the invention and may moreover result in reduced requirements with respect to noise shaping of the intersections if the intersections are noise shaped prior to
15 transformation into the common time domain.

Fig. 17 illustrates an exemplary circuit used for the purpose of establishment of an output PWM signal. If true differential three-level output is needed, two of the illustrated circuits are needed. In the illustrated embodiment, two edge-determining
20 words W1 and W2 are loaded to the counter circuit. W1 determines the first edge of the signal and W2 determines the second edge and the illustrated output PWM A-signal.

Fig. 18 illustrates a timing diagram of an embodiment of the invention in which two
25 edge-determining data words, - e.g. established in the basis of the above-described method according to an embodiment of the invention. The words are then, e.g. by means of a counter-circuits of the above-described kind, established in the following period, PWM CUR.

30 The corresponding timing diagram is illustrated in fig. 18.